CLAIMS

Sub A'

1. A voltage doubler receiving at an input a continuous power voltage and supplying at an output a voltage having a value virtually double that of said continuous power voltage, the voltage doubler comprising:

a. an oscillator, powered by said continuous power voltage having a first output, and a second output in phase opposition to the first output,

b. a charge accumulation capacitor having a first terminal connected to a potential reference and a second terminal connected to the output of the doubler,

c. a first charge transfer capacitor having a first terminal connected to said first output of said oscillator, and

d. two inverters connected together in a loop so as to form a flip-flop having a first input connected to a second terminal of said first capacitor , negative power terminals connected together to said continuous power voltage and positive power terminals connected together to said second terminal of said charge accumulation capacitor, and

e. a second charge transfer capacitor having a first terminal connected to said second output of said oscillator and a second terminal connected to a second input of said inverters.

2. The voltage doubler in accordance with claim 1, wherein said inverters include MOS transistors which are virtually equal, and wherein corresponding bulk terminals of said MOS transistors are connected in such a manner as to create a one-way conduction path between said negative terminals and said positive terminals of said inverters.

3. A voltage doubler receiving at an input a continuous power voltage and supplying at an output a voltage having a value virtually double that of said continuous power voltage, the voltage doubler comprising:

a. an oscillator powered by said continuous power voltage and having two outputs in phase opposition,

b. a charge accumulation capacitor having a first terminal connected to a potential reference and a second terminal connected to the output of the doubler,

c. a first charge transfer capacitor and a second charge transfer capacitor having first terminals respectively connected to the outputs of said oscillator,

d. a bridge comprising four diodes, having a positive terminal connected to the second terminal of said charge accumulation capacitor, a negative terminal connected to said continuous power voltage and two indifferent terminals respectively connected to second terminals of said first charge transfer capacitor and said second charge transfer capacitor, and

e. four transistors having principal conduction paths connected in parallel with said four diodes and control terminals connected in such a way as to lower the voltage drop along the bridge branches at steady state.

4. The voltage doubler in accordance with claim 3, wherein said four transistors are MOS type and are virtually equal.

5. The voltage doubler in accordance with claim 3, wherein said four diodes are respective bulk diodes of said four transistors.

6. A voltage booster receiving at an input a continuous power voltage and supplying at an output a voltage higher than the continuous power voltage, the voltage booster comprising:

a. an oscillator powered by said continuous power voltage, having two outputs in phase opposition,

b. a charge accumulation capacitor having a first terminal connected to a first potential reference and a second terminal connected to the output of the booster, and

c. at least one charging section having a charge output terminal, a power input terminal, a first side terminal and a second side terminal respectively connected to the outputs of said oscillator, and said at least one charging section being connected in series with the output terminal connected to the second terminal of said charge accumulation capacitor and the input terminal connected to a continuous power voltage,

wherein the at least one charging section comprises:

a first charge transfer capacitor and a second charge transfer capacitor having respective first terminals connected to said first and second side terminals, and

a bridge of controlled switches having two indifferent terminals connected to respective second terminals of said first charge transfer capacitor and said second charge transfer capacitor, a negative terminal connected to said power input terminal and a positive terminal connected to said charge output terminal ,

and wherein the value of the voltage of the output corresponds to said second potential less the value of said first potential plus the product of said continuous power voltage and a number of the at least one charging section.

7. The voltage booster in accordance with claim 6, wherein the switches of said bridge form two inverters connected together in a loop so as to form a flip-flop, having inputs connected to respective second terminals of said first charge

transfer capacitor and said second charge transfer capacitor, negative power terminals connected together to said power input terminal and positive power terminals connected together to said charge output terminal.

8. The voltage booster in accordance with claim 7, wherein said switches include MOS transistors.

9. The voltage booster in accordance with claim 8, wherein corresponding bulk terminals of said MOS transistors are connected in such a way as to create a one-way conduction path between said power input terminal and said charge output terminal.

10. The voltage booster in accordance with claim 7, wherein said inverters are virtually equal.

11. The voltage booster in accordance with claim 6, wherein said first input terminal is connected to said continuous power voltage.

12. The voltage booster in accordance with claim 6, wherein said oscillator provides a single output from an inverting buffer and from a non-inverting buffer having virtually equal delays.

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13. An electrically programmable and delectable non-volatile memory device of the type powerable with low voltage comprising:

a. an oscillator powered by said continuous power voltage, having two outputs in phase opposition;

b. a charge accumulation capacitor having a first terminal connected to a first potential reference and a second terminal connected to the output of the booster, and

c. at least one charging section having a charge output terminal, a power input terminal, a first side terminal and a second side terminal respectively connected to the outputs of said oscillator and said at least one charging section being connected in series with the output terminal connected to the second terminal of said charge accumulation capacitor and the input terminal connected to a continuous power voltage,

wherein the at least one charging section comprises:

a first charge transfer capacitor and a second charge transfer capacitor having respective first terminals connected to said first and second side terminals, and

a bridge of controlled switches having two indifferent terminals connected to respective second terminals of said first charge transfer capacitor and said second charge transfer capacitor, a negative terminal connected to said power input terminal and a positive terminal connected to said charge output terminal ,

and wherein the value of the voltage of the output corresponds to said second potential less the value of said first potential plus the product of said continuous power voltage and a number of the at least one charging section.

14. A voltage regulator having a low voltage drop between an input and an output of the type having a MOS power transistor as an output regulation element and a voltage booster means having output coupled to a control terminal of said power transistor to hold said transistor in conduction condition with changes in the operating conditions of the regulator, wherein the voltage booster means includes:

a. an oscillator powered by said continuous power voltage, having two outputs in phase opposition,

b. a charge accumulation capacitor having a first terminal connected to a first potential reference and a second terminal connected to the output of the booster, and

c. at least one charging section having a charge output terminal, a power input terminal, a first side terminal and a second side terminal respectively connected to the outputs of said oscillator and said at least one charging section being connected in series with the output terminal connected to the second terminal of said charge accumulation capacitor and the input terminal connected to a continuous power voltage,

wherein the at least one charging section comprises:

a first charge transfer capacitor and a second charge transfer capacitor having respective first terminals connected to said first and second side terminals, and

a bridge of controlled switches having two indifferent terminals connected to respective second terminals of said first charge transfer capacitor and said second charge transfer capacitor, a negative terminal connected to said power input terminal and a positive terminal connected to said charge output terminal ,

and wherein the value of the voltage of the output corresponds to said second potential less the value of said first potential plus the product of said continuous power voltage and a number of the at least one charging section.

15. A voltage multiplier receiving a constant voltage comprising:

an oscillator providing two outputs in phase opposition;

multiplying means connected to the constant voltage and the oscillator outputs for generating a multiplied voltage which is a multiple of the constant voltage; and

output means receiving the multiplied voltage for outputting a substantially constant output voltage which is a multiple of the constant voltage.

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16. The voltage multiplier of claim 15, wherein the output means includes a charge accumulation capacitor connected between the multiplied voltage and a potential reference.

17. The voltage multiplier of claim 16, wherein the output voltage is outputted at the connection between the charge accumulation capacitor and the multiplied voltage.

18. The voltage multiplier of claim 15, wherein the oscillator is powered by the constant voltage.

19. The voltage multiplier of claim 15, wherein the multiplying means includes:

at least one first charge transfer capacitor connected to one output of the oscillator;

at least one second charge transfer capacitor connected to another output of the oscillator;

at least one bridge circuit having an input coupled to the constant voltage, an output providing the multiplied voltage, and at least two side inputs respectively coupled to the at least one first charge transfer capacitor and the at least one second charge transfer capacitor.

20. The voltage multiplier of claim 19, wherein:

the at least one first charge transfer capacitor includes a plurality of first charge transfer capacitors, each being connected to one output of the oscillator;

the at least one second charge transfer capacitor includes a plurality of second charge transfer capacitors corresponding to the plurality of first charge transfer capacitors, each of the second charge transfer capacitors being connected to another output of the oscillator;

the at least one bridge circuit includes a plurality of series connected bridge circuits corresponding to the plurality of first charge transfer capacitors and plurality of second charge transfer capacitors, each bridge circuit having two side

inputs connected to a respective first charge transfer capacitor and a respective second charge transfer capacitor.

21. The voltage multiplier of claim 19, wherein the at least one bridge circuit includes:

four diodes in a bridge arrangement such that a positive terminal is the output, a negative terminal is the input, and two indifferent terminals are the side inputs; and

four transistors having principal conduction paths connected in parallel with the four diodes and control terminals connected to the side inputs.

22. The voltage multiplier of claim 20, wherein each of the plurality of series connected bridge circuits includes:

four diodes in a bridge arrangement such that a positive terminal is the output, a negative terminal is the input, and two indifferent terminals are the side inputs; and

four transistors having principal conduction paths connected in parallel with the four diodes and control terminals connected to the side inputs.

23. A method for generating an output voltage based upon a lower constant input voltage comprising the steps of:

generating a first periodic signal;

generating a second periodic signal out of phase to said first periodic signal;

applying the first periodic signal to at least one first charge transfer capacitor;

applying the second periodic signal to at least one second charge transfer capacitor;

generating said output voltage based upon said input voltage, an output voltage of the at least one first charge transfer capacitor, an output voltage of the at least one second charge transfer capacitor.

24. The method of claim 23, the step of generating the output voltage includes the steps of:

applying said input voltage, an output voltage of the at least one first charge transfer capacitor, an output voltage of the at least one second charge transfer capacitor to inputs of a bridge circuit;

applying an output of the bridge circuit to a first terminal of a charge accumulation capacitor, a second terminal of the charge accumulation capacitor being connected to a potential reference; and

providing said output voltage at said first terminal of the charge accumulation capacitor.

25. The method of claim 23, wherein:

the first periodic signal is applied to a plurality of first charge transfer capacitors;

the second periodic signal is applied to a plurality of second charge transfer capacitors; and

the generating step includes:

applying respective outputs of the plurality of first charge transfer capacitors and respective outputs of the plurality of second charge transfer capacitors as inputs to a respective plurality of bridge circuits arranged in a series;

applying the input voltage to an input of a first in the series of the plurality of bridge circuits; and

providing an output of a last in the series of the plurality of bridge circuits as the output voltage.